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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,829	04/06/2001	Magnus Karlsson	TI-32581	6359

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EXAMINER	
HO, CHUONG T	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,829	KARLSSON ET AL.	
	Examiner	Art Unit	
	Chuong Ho	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-24 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 13, 2-8, 10-12, 14-20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dighe et al. (U.S.Patent No. 5,717,691) in view of Hwang (U.S.Patent No. 2002/0080821 A1 "Filed April 03, 2001").

In the claim 1, Dighe et al. discloses ATM module (engine 25) comprising: a plurality of data ports (115) operably configured to transceiver telecommunications traffic across a local area network and wire area network (see col. 10, lines 5-7, the main components of the engine include a bus interface and the ATM SAR chip);

A function module (AAL1 Engine, AAL ¾ Engine) operably configured to transceiver ATM adaptation layer (AAL) type traffic (see figure 5, three set of engine units are included, one for the AAL 1 (103, 106) protocol, one for the AAL ¾ (104, 107) protocol, and a third MAAL (105, 108) for the future AAL2 (or video) protocol, for each of the transmit and receive function);

An ATM processor (EPROM 113) coupled to each of data ports (bus interface 101) and function module (AAL1 Engine, AAL ¾ Engine) and operably configured to switch ATM data cells to and from data ports (bus 101) and function module (AAL1 Engine, AAL ¾ Engine), switching including traffic flow between one of data ports (bus 101) and

function module (AAL1 Engine, AAL ¾ Engine) and between two of data ports (bus 101) (see col. 10, lines 21-25, EPROM 113 is coupled to state memory 110 to serve as a table lookup for video concealment support of the multimedia AALs 105, 108. A synchronous residual time stamp clock recovery circuit 114 is included coupled to AAL-1 engine as is customary);

A cell buffer module coupled to ATM processor (EPROM 113) and operably configured to buffer ATM data cells for supporting traffic transmission control between data ports (bus 101) and function module (AAL1 Engine, AAL ¾ Engine), wherein function module (AAL1 Engine, AAL ¾ Engine), ATM processor (EPROM 113), and cell buffer module (state memory 109) (see col. 10, lines 13-19, an SRAM 109 that serves as the state memory interface is coupled to the sequencer by way of the state memory interface unit 111 for receiving various control signals from the router. A one cell buffer 112 is interposed between the bus interface unit and the sequencer for temporary storage).

However, Digle is silent to disclosing an asynchronous transfer mode (ATM) module interfacing with a network processing unit .

Hwang discloses an asynchronous transfer mode (ATM) module (ATM SAR MODULE 700) interfacing with a network processing unit (processor 704) (see figure 7); cell buffer module (packet memory 707) are further configured to interface with network processing unit (processor 704) (see figure 7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Digle with the teaching of Hwang to provide an

asynchronous transfer mode (ATM) module interfacing with a network processing unit in order to improving efficiency for data transmission and reception.

3. In the claim 13, Dighe et al. discloses ATM switching module (engine 25) comprising: a plurality of data ports (115) operably configured to transceiver telecommunications traffic across a local area network and wire area network (see col. 10, lines 5-7, the main components of the engine include a bus interface and the ATM SAR chip);

A function module (AAL1 Engine, AAL ¾ Engine) operably configured to transceiver ATM adaptation layer (AAL) type traffic (see figure 5, three set of engine units are included, one for the AAL 1 (103, 106) protocol, one for the AAL ¾ (104, 107) protocol, and a third MAAL (105, 108) for the future AAL2 (or video) protocol, for each of the transmit and receive function);

An ATM processor (EPROM 113) coupled to each of data ports (bus interface 101) and function module (AAL1 Engine, AAL ¾ Engine) and operably configured to switch ATM data cells to and from data ports (bus 101) and function module (AAL1 Engine, AAL ¾ Engine), switching including traffic flow between one of data ports (bus 101) and function module (AAL1 Engine, AAL ¾ Engine) and between two of data ports (bus 101) (see col. 10, lines 21-25, EPROM 113 is coupled to state memory 110 to serve as a table lookup for video concealment support of the multimedia AALs 105, 108. A synchronous residual time stamp clock recovery circuit 114 is included coupled to AAL-1 engine as is customary);

A cell buffer module coupled to ATM processor (EPROM 113) and operably configured to buffer ATM data cells for supporting traffic transmission control between data ports (bus 101) and function module (AAL1 Engine, AAL ¾ Engine), wherein function module (AAL1 Engine, AAL ¾ Engine), ATM processor (EPROM 113), and cell buffer module (state memory 109) (see col. 10, lines 13-19, an SRAM 109 that serves as the state memory interface is coupled to the sequencer by way of the state memory interface unit 111 for receiving various control signals from the router. A one cell buffer 112 is interposed between the bus interface unit and the sequencer for temporary storage). However, Digle is silent to disclosing an asynchronous transfer mode (ATM) switching module interfacing with a network processing unit .

Hwang discloses an asynchronous transfer mode (ATM) switching module (ATM SAR MODULE 700) interfacing with a network processing unit (processor 704) through an interface system, wherein host processing unit initializes configuration of ATM switching module (ATM SAR MODULE 700) via interface system (see figure 7) ; cell buffer module (packet memory 707) are further configured to interface with network processing unit (processor 704) (see figure 7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Digle with the teaching of Hwang to provide an asynchronous transfer mode (ATM) module interfacing with a network processing unit in order to improving efficiency for data transmission and reception.

4. In the claims 2, 14, Hwang discloses at least one of data ports is an UTOPIA level 2 port and one data ports is a broadband port (see figure 7, page 2, [0021], a

UTOPIA interface controller providing a standard connection between the ATM SAR and a physical module, [0042]).

5. In the claims 3, 15, Hwang discloses UTOPIA level-2 port is configured to interface with an ATM 25 LAN and Broadband port is configured to interface with a DSL modem (see [0004], a conventional xDSL communication service chip for directly sharing a communication match with each subscriber at the small office or home and providing various communication services, such as internet TV).

6. In the claims 4, 16, Hwang discloses UTOPIA level-2 port is further configured to interface with Broadband port (see figure 7, page 2, [0021], a UTOPIA interface controller providing a standard connection between the ATM SAR and a physical module, [0042]).

7. In the claims 5, 17, Digle discloses one of data ports is a LAN interface via an interconnect bus (see col. 10, lines 5-7, the main components of the engine include a bus interface and the ATM SAR chip);

8. In the claims 6, 7, 8, 18, 19, 20, Digle discloses function module includes an AAL2 type module and an AAL5 type module (see figure 5, three set of engine units are included, one for the AAL 1 (103, 106) protocol, one for the AAL ¾ (104, 107) protocol, and a third MAAL (105, 108) for the future AAL2 (or video) protocol, for each of the transmit and receive function).

9. In the claims 10, 22, Hwang discloses ATM data cells are buffered via cell buffer module (packet memory 707) for switching from a high-speed data port to a low-speed data port (see page 2, [0021] [0022]).

10. In the claims 11, 23, Hwang discloses ATM processor (ATM SAR MODULE) is further configured to enable quality or service, and operation and maintenance processing (see page 1, [0006], an optimum data exchange in the ATM SAR between the suppliers and consumers of the information and the ATM SAR, is an important factor to decide an efficiency of the xDSL communication chip and a service quality provided to users).

11. In the claims 12, 24, Hwang discloses ATM processor is further configured to enable virtual paths cross-connect and virtual channel identifier/virtual path identifier traffic flows (see page 2, [0014], the configuration in FIG.4 controls table information according to a VPI (Virtual Path Identifier) and a VCI (Virtual Channel Identifier) of the ATM virtual channel which an user demands. The data inputted and outputted through a path of the virtual channel are shared through a host bus and a large capacity memory).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined system (Digle - Hwang) in view of Li et al. (U.S.Patent No.I 2003/0076839 A1).

In the claims 9, 21, the combined system (Digle – Hwang) discloses the limitations of claim 1 above.

However, the combined system (Digle – Hwant) is silent to disclosing ATM processor is configured to act as the only master and data ports, function module, and cell buffer are configured to act as slaves.

Li et al. discloses a slave interface unit controls the exchange of data between a master processing unit (ATM processor) and a plurality of slave processing units (data ports, function module, and cell buffer) operating in the asynchronous transfer mode (ATM) of operation (see abstract, figure 3).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Digle – Hwant) with the teaching of Li to provide a slave interface unit controls the exchange of data between a master processing unit (ATM processor) and a plurality of slave processing units (data ports, function module, and cell buffer) operating in the asynchronous transfer mode (ATM) of operation in order to facilitate the exchange of data there between.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong ho whose telephone number is (571)272-3133. The examiner can normally be reached on Monday-Friday from 8:00AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/05/04